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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,913	07/29/2003	Yeen Tat Chan	CS02-068	8122

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EXAMINER	
DANG, TRUNG Q	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,913	CHAN ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-44 is/are pending in the application.

4a) Of the above claim(s) 23-44 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/29/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of the Group II invention, claims 1-22 in the reply filed on 8/11/04 is acknowledged. The traversal is on the ground(s) that the fields of search for the Group I and Group II inventions are clearly and necessarily co-extensive. This is not found persuasive because of the followings:

With regard to applicants' allegation that the fields of search for the Group I and Group II inventions are clearly and necessarily co-extensive. This is found unconvincing because the issues of product and method claims are divergent. There may be some overlap in the searches of the two groups, but there is no reason to believe that the searches would be identical. Furthermore, the examination of the process claims is based on different criteria from that of the device claims, hence the examination of the two groups is not co-extensive. Therefore, based on the additional work involved in searching and examination of the two distinct inventions together that would present serious burden to the examiner, restriction of distinct invention is clearly proper.

With regard to applicants' allegation that process proposed by the examiner is very speculative and really has nothing to do with the claims as presented in this application. Such allegation is found unpersuasive because the examiner has clearly presented a materially different process that would produce the claimed product. Of course, the proposed process has nothing to do with the claims as presented in this application because the proposed process is materially different from the pending process claims. The purpose of presenting the proposed process is to demonstrate that the product as claimed can be made by another materially different process (M.P.E.P §806.05(f)). In this regard, applicants have failed to point out as to why the proposed process would not render the claimed product.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S. Pat. 6,521,959 cited by applicants) in view of Arisumi et al. (U.S. Pat. 5,886,385).

With reference to Fig. 5 and Figs. 6A-11C, Kim teaches a method of forming a metal oxide semiconductor field effect transistor (MOSFET) device on a semiconductor substrate, comprising the steps of:

providing a supporting substrate 53;

forming a silicon on insulator (SOI) layer 1 on said substrate (Fig. 6A);

forming shallow trench isolation regions (STI) 3a and 3b including an oxide filled STI region 3b in the silicon component of the SOI layer, with depth of said STI 3b terminating at the top surface of the insulator component 51 of said SOI layer (Fig. 9A);

forming a gate insulator layer 65 on surface of said silicon component of said SOI layer;

forming a conductive gate structure 5 on said gate insulator layer, and on portions of said STI regions 3a and 3b (Fig. 10A);

forming a body contact region 1b (Fig. 5) in a first portion of said silicon component of said SOI layer; and

forming a source/drain region (1s/1d) in a second portion of said silicon component of said SOI layer, wherein said second portion of said silicon

component of said SOI layer is separated from said first portion of said silicon component of said SOI layer by said STI region 3b.

Noted the followings:

a) The insulator isolation layer comprises STI regions 3a and 3b reads on the claimed STI region because the insulator isolation layer includes STI region 3b with depth terminating at the top surface of the insulator component 51 of said SOI layer.

b) As shown in Fig. 5, the gate structure 5 extends over portion of STI region 3a, hence the claimed limitation "forming a conductive gate structure on said gate insulator layer, and on portions of said STI regions" is anticipated by the reference because the STI region 3a is a part of the insulator isolation layer.

c) The body line 1b where a body contact is formed thereon reads on the claimed limitation "body contact region", and the body line1b is formed on a first portion of the silicon layer 1; the second portion of the silicon layer 1 is the active region in which source region 1s and drain region 1d are formed (Fig. 5)

d) Not shown in Fig. 5, the insulator isolation layer covers the entire surface of the structure of Fig. 5 (col.9, lines 22-28), rendering the second portion of the silicon layer 1 (source/drain portion) is separated from the first portion of the silicon layer 1 (body line portion) by said insulator isolation layer (see the insulator isolation layer fills the trench portion between source/drain 1s/1d and body line 1).

Kim differs from the claims in that while Kim discloses a supporting substrate 53 for the SOI layer, the claims call for a p-type semiconductor substrate for the SOI layer. Arisumi shows in a typical SOI technology, however, a p-type semiconductor substrate is widely used for supporting an SOI layer formed thereon (Fig. 5B). Thus, it would have been obvious to one of ordinary skill in the art to use a p-type semiconductor substrate as the support substrate in Kim's process because

such is widely practice in the art, and the application of a known material to make the same would have been within the level of an artisan, absent any showing of criticality by applicants.

For claim 5, since the insulator isolation layer reads on the claimed STI region for reason a) noted above and covers the entire surface of the structure of Fig. 5, the area of the insulator isolation layer is obviously within the claimed range as clearly shown in Fig. 5.

4. Claims 3, 4, 6, 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. taken with Arisumi et al. as applied to claims 1,2,5,7 above, and further in view of Hirano (US. Pat. 6,37,230).

The combination of Kim and Arisumi teaches a method of forming a MOSFET device on an SOI substrate as described above. The combined process differs from the claims in not disclosing numerical values for elements of the MOSFET device as recited in claims. Hirano teaches a method of forming a MOSFET device on an SOI substrate, which includes the following process parameters: a buried oxide film 3 (corresponding to the insulator component recited in claim 3) with a thickness of 4,000 Å (col. 6, line 24-26); a SOI layer 4 with a thickness of several thousand angstroms (e.g., 2,000 Å) (col. 6, lines 26-27); a gate oxide film 5 with a thickness of several tens of angstroms (e.g., 50 Å) (col. 6, lines 59-60); a polysilicon gate structure with a thickness of several thousand angstroms (e.g., 2,000 Å); n-type source/drain region for NMOS device obtained via implantation of arsenic ions at an energy between about 10 to 50 KeV, at a dose between about 1E15 to 5E15 atoms/cm^2 (col. 10, lines 62-63); p-type source/drain region for PMOS device obtained via implantation of boron or BF_2 ions at an energy between about 10 to 50 KeV, at a dose between about 1E15 to 5E15 atoms/cm^2 (col. 10, lines 63-65). Thus, it would have been obvious to one of ordinary skill in the art to form the gate oxide, the polysilicon gate, the n-type source/drain, and the p-type

source/drain of the combined teaching by employing the numerical values as taught in Hirano because such values are typical in the art of making NMOS and/or PMOS devices on a SOI substrate, and the application of a known set of values to made the same would have been within the level of one skilled in the art.

As for claims 3, although the thickness value of the buried oxide of the claim is different from that of disclosed by Hirano, it is well settle that, absent a showing of criticality by applicant, the determination of the claimed thickness would have been obvious to one of ordinary skill in the art since it has been held that, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and In re Geisler, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997).

As for claim 11, although Kim teaches implantation of an n-type impurity into the body line 1b in order to form a body line 1b having a relatively low resistance (col. 10, lines 31-33 in conjunction with col. 7, lines 24-33), Kim is silent about the energy and doses for the implantation. However, the determination of such parameters would have been obvious to one having ordinary skill in the art since it has been held that, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and In re Geisler, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 12-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The last step of independent claim 12 recites "forming N type or P type source/drain region in an area of said first portion of said silicon layer not covered by said polysilicon gate structure not covered by said polysilicon gate structure for a P channel device." The step of forming N type **or** P type source/drain region indicates either NMOS device or PMOS device is formed but not both. Nevertheless, the claim appears to have two polysilicon gate structures including the polysilicon gate structure for a P channel device that lacks antecedent basis, which renders the claim so ambiguous and cannot be understood. Since the scope of independent claim 12 cannot be ascertained, a rejection over prior art cannot be made at this time.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

09/22/04